AMENDMENTS TO THE CLAIMS:

Please cancel without prejudice claim 19, amend claims 1-6, 8, 9, 12-16, 21, 23 and 24 and add newly written claim 32 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A method of generating ~~pulsed~~ first and second switching signals for switching first and second switches of a switching circuit that further ~~comprising~~ comprises an output ~~and~~ that receives a DC ~~signal~~ supply of nominal voltage $+V_S$, and wherein switching between various combinations of on and off states of the first and second switches produces a voltage at the output with pulses at levels of $+V_S$, 0V and $-V_S$;

the method comprising the steps of:

(a) receiving a voltage demand signal indicative of a desired voltage to be supplied at the output in a period; and

(b) generating the first and second switching signals, wherein at least one of ~~according to a first rule that~~ the first and second switching signals ~~shall have~~comprises a single pulse of a ~~first~~ determined width within the period, wherein the determined ~~and, subject to a second rule that the pulse~~ width ~~of the resulting voltage at the output~~ does ~~must~~ not fall below a minimum pulse width, and further, wherein successive transitions between on and off states of the first switching signal or of the second switching signal that occur in different periods are separated in time by a minimum time period, ~~that the second switching signal shall remain in one state throughout the period;~~and wherein the ~~first~~ determined width ~~being~~ is such that the combination of the first and second switching signals when applied to the first and second switches respectively produce an

average voltage at the output for the period ~~being~~ that is substantially equal to the desired voltage.

2. (currently amended) The method of claim 1, wherein, ~~comprising the~~ at step b), the first switching signal comprises a single pulse of a first determined width within the period and ~~of generating the first and second switching signals according to a rule that pulse widths below the minimum pulse width are avoided by departing from the rule that the second switching signal shall remain in one state throughout a period in favour of a rule that~~ the second switching signal ~~shall have~~comprises a single pulse of a second determined width within the period, wherein neither said first nor said second determined width falls below said minimum pulse width and wherein said first and second determined widths are such that the combination of the first and second switching signals when applied to the first and second switches respectively produce an average voltage at the output for the period that is substantially equal to the desired voltage ~~to create a voltage pulse at the output of either $+V_S$ or $-V_S$~~.

3. (currently amended) The method of claim 2, further comprising the step of ~~adding~~ increasing the ~~second~~ first determined width by an amount that is equal in magnitude to the ~~first~~ second determined width but compensatory in effect in ~~such~~ that ~~the~~ a voltage pulse at the output of $+V_S$ or $-V_S$ resulting from the pulse in the second switching signal is balanced by an equal width of voltage pulse at the output of $-V_S$ or $+V_S$ respectively resulting from the increased first determined width of the first switching signal.

4. (currently amended) The method of claims 2, further comprising the step of generating the first and second switching signals according to a rule that the leading and trailing edges of the first switching signal do not coincide with either the leading or trailing edge of the second switching signal.

5. (currently amended) The method of claim 1, further comprising the step of generating the first and second switching signals according to a rule that any pulse should be positioned symmetrically about the centre of the period.

6. (currently amended) The method of claim ~~5~~1, further comprising the step of generating the first and second switching signals according to the rule that where pulses cannot be centred symmetrically, the longer and shorter sides of the asymmetric pulses are alternated between the leading edge side and the trailing edge side for successive asymmetric pulses.

7.(previously presented) The method of claim 1 further comprising the step of noise shaping the first and second switching signals.

8. (currently amended) A method of operating a switching circuit comprising a bridge circuit having an input that receives a DC ~~signal~~ supply of nominal voltage $+V_S$, an output and first and second arms having first and second switches respectively, the first and second arms being connected to opposed ends of the output,

the method comprising the steps of:

(a) generating pulsed first and/or second switching signals in accordance with ~~any preceding~~ claim 1; and

(b) supplying the first and second switching signals to the first and second switches respectively thereby to cause the first and second switches to switch between on and off states, switching between various combinations of on and off states producing an electrical signal across the output with voltage pulses at levels of $+V_S$, 0V and $-V_S$ and with an average voltage for the period substantially equal to the desired voltage.

9. (currently amended) The method of claim 8, wherein either the first or second determined pulse width is generated with reference to a voltage signal indicative of the DC ~~signal~~ supply voltage such that the determined pulse width compensates for fluctuations in the DC supply.

10. (currently amended) The method of claim 9, wherein the voltage signal is passed through a filter to obtain a predictive measure of fluctuations in the DC supply.

11. (original) The method of claim 10, wherein the voltage signal is passed through a finite impulse response filter.

12. (currently amended) The method of claim 8, wherein either the first or second determined pulse width is generated to include ~~additional~~ an adjustment to the width of the pulse to compensate for a voltage drop across a diode and/or transistor in the bridge circuit.

13. (currently amended) The method of claim 12, wherein the ~~additional~~ adjustment to the pulse width is calculated with reference to a current signal indicative of the current flowing through the output and to a representative resistance of the diode or transistor.

14. (currently amended) The method of claim 8, wherein ~~the width of~~ a pulse of the first or second switching signals is generated to include ~~additional~~ an adjustment to the width of the pulse to compensate for a voltage offset caused by a slow response ~~times~~ in generating the first or second switching signals.

15. (currently amended) The method of claim 1, wherein the first and second switches are transistors and the method comprises the step of switching the transistors between on and off states corresponding to substantially ~~maximum~~ minimum voltage drop and substantially minimum current flow respectively through the transistors.

16. (currently amended) The method of claim 1, further comprising the step of receiving a current demand signal indicative of a desired current to be supplied to the output in a period and calculating the voltage demand signal indicative of a desired voltage to be supplied to the output that results in an electrical signal being supplied to the output during the period with a current substantially equal to the desired current.

17. (original) The method of claim 16, wherein the step of calculating the voltage demand signal is performed with reference to a model of the load characteristic of a load connected to the output.

18. (previously presented) The method of claim 16 further comprising the step of generating the voltage demand signal with reference to a current signal indicative of the current flowing through the output.

19. (cancelled).

20. (previously presented) A computer program product comprising program code means stored on a computer readable medium for performing the method steps of claim 1 when the program is run on a computer and/or other processing means associated with the switching circuit.

21. (currently amended) A switching circuit operable to receive a DC ~~signal~~ supply of nominal voltage $+V_S$ and that comprises first and second switches, an output and processing means programmed to perform the method steps of claim 1.

22. (original) A switching circuit according to claim 21, further comprising a noise shaper operable to noise shape the first and second switching signals.

23. (currently amended) A bridge circuit comprising an input operable to receive a DC ~~signal~~ supply of nominal voltage $+V_S$, an output and first and second arms having first and second switches respectively, the first and second arms being connected to opposed ends of the output and processing means programmed to perform the method steps of claim 8.

24. (currently amended) A bridge circuit ~~according to claim 23~~comprising an input operable to receive a DC supply of nominal voltage $+V_S$, an output and first and second arms having first and second switches respectively, the first and second arms being connected to opposed ends of the output, further comprising a voltage signal sensor operable to produce a voltage signal and wherein the processing means is programmed to perform the method steps of claim 9.

25. (original) A bridge circuit according to claim 24, further comprising a filter arranged to receive the voltage signal.

26. (original) A bridge circuit according to claim 25, wherein the filter is a finite impulse response filter.

27-31 (cancelled).

32. (new) The method of claim 1, wherein, at step b), the first switching signal comprises a pulse of the determined width within the period and the second switching signal remains in one state throughout the period.